**Institute of Engineering & Management**

**Department of Computer Science & Engineering**

**Computer Architecture Laboratory for 2nd year 4th semester 2018**

**Code: CS 493**

**Date:** 24/02/2018

**WEEK-5**

**Assignment:** Implementation of encoders and decoders Binary using Xilinx ISE.

**Objective:**  Implement 2:4 decoder using case.

|  |  |
| --- | --- |
| **Property Name** | **Value** |
| Device family | Spartan 3 |
| Device | XC3S50 |
| Package | PQ208 |
| Speed | -5 |
| Top-level source type | HDL |
| Synthesis Tool | XST(VHDL/Verilog) |
| Simulator | ISE Simulator |
| Preferred Language | VHDL |

**Software used:**

**Theory:**

1. Make VHDL with required port specification.
2. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
3. Make test bench waveform and check for the given inputs.

**Truth Table:**

|  |  |
| --- | --- |
| **Input** | **Output** |
| 00 | 0001 |
| 01 | 0010 |
| 10 | 0100 |
| 11 | 1000 |

**Code:**

**Using Case:**

entity a2 is

Port ( a : in STD\_LOGIC\_VECTOR (1 downto 0);

b : out STD\_LOGIC\_VECTOR (3 downto 0));

end a2;

architecture Behavioral of a2 is

begin

process(a)

begin

case a is

when "00"=> b<="0001";

when "01"=> b<="0010";

when "10"=> b<="0100";

when "11"=> b<="1000";

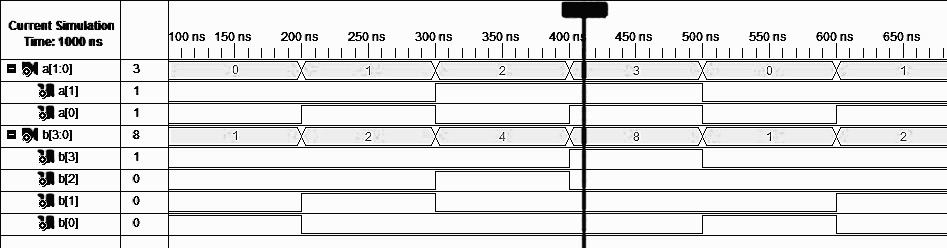
when others=> b<="XXXX";

end case;

end process;

end Behavioral;

**Output:**

****

**Objective:**  Implement 4:2 encoder using data flow and case loop.

|  |  |
| --- | --- |
| **Property Name** | **Value** |
| Device family | Spartan 3 |
| Device | XC3S50 |
| Package | PQ208 |
| Speed | -5 |
| Top-level source type | HDL |
| Synthesis Tool | XST(VHDL/Verilog) |
| Simulator | ISE Simulator |
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**Software used:**

**Theory:**

1. Make VHDL with required port specification.
2. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
3. Make test bench waveform and check for the given inputs.

**Truth Table:**

|  |  |
| --- | --- |
| **Input** | **Output** |
| 0001 | 00 |
| 0010 | 01 |
| 0100 | 10 |
| 1000 | 11 |

**Data flow Model:**

**Code:**

**Data flow:**

entity a2 is

Port ( a : in STD\_LOGIC\_VECTOR (3 downto 0);

b : out STD\_LOGIC\_VECTOR (1 downto 0));

end a2;

architecture Behavioral of a2 is

begin

b(1)<= a(3) or a(2);

b(2)<= a(3) or a(1);

end Behavioral;

**Using Case:**

entity a2 is

Port ( a : in STD\_LOGIC\_VECTOR (3 downto 0);

b : out STD\_LOGIC\_VECTOR (1 downto 0));

end a2;

architecture Behavioral of a2 is

begin

process(a)

begin

case a is

when "0001"=> b<="00";

when "0010"=> b<="01";

when "0100"=> b<="10";

when "1000"=> b<="11";

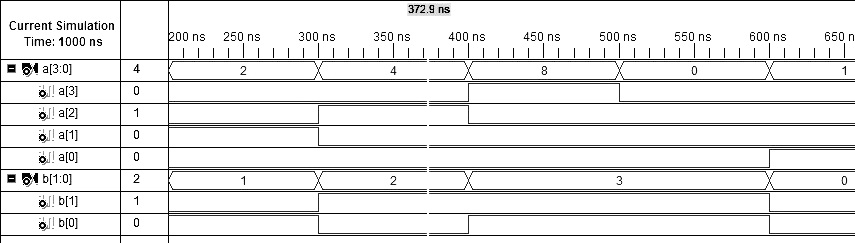
when others=> b<="XXXX";

end case;

end process;

end Behavioral;

**Output:**

****

**Objective:**  Implement 8:3 encoder using for loop.

|  |  |
| --- | --- |
| **Property Name** | **Value** |
| Device family | Spartan 3 |
| Device | XC3S50 |
| Package | PQ208 |
| Speed | -5 |
| Top-level source type | HDL |
| Synthesis Tool | XST(VHDL/Verilog) |
| Simulator | ISE Simulator |
| Preferred Language | VHDL |

**Software used:**

**Theory:**

1. Make VHDL with required port specification.
2. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
3. Make test bench waveform and check for the given inputs.

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Input** | **Output** |  | **Input** | **Output** |
| 00000001 | 000 |  | 00010000 | 100 |
| 00000010 | 001 |  | 00100000 | 101 |
| 00000100 | 010 |  | 01000000 | 110 |
| 00001000 | 011 |  | 10000000 | 111 |

**Behavioral Model:**

**Code:**

**Behavioral Model:**

entity a1 is

Port ( a : in STD\_LOGIC\_VECTOR (7 downto 0);

b : out STD\_LOGIC\_VECTOR(2 downto 0));

end a1;

architecture Behavioral of a1 is

begin

process(a)

variable d : INTEGER;

begin

for i in 0 to 7 loop

if a(i)='1' then

d:=i;

end if;

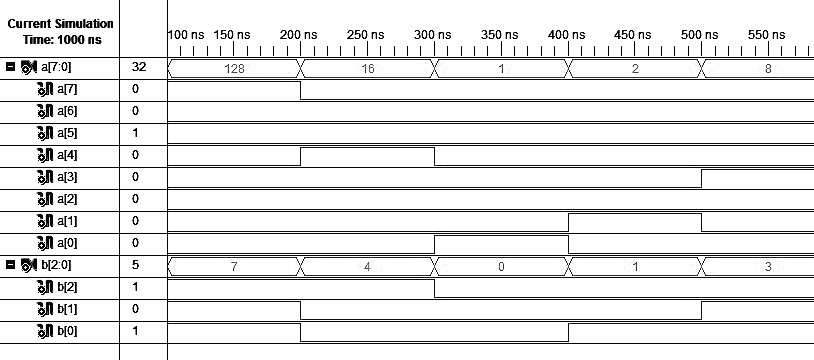
end loop;

b<=conv\_STD\_LOGIC\_VECTOR(d,3);

end process;

end Behavioral;

**Output:**

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